IN THE CLAIMS:

Please amend the claims as indicated below:

1. (Currently Amended) A method for determining characteristics of metal oxide semiconductor (MOS) devices, the method comprising the steps of:

providing a plurality of ring oscillators, the plurality of ring oscillators located within a predetermined distance of one another, each ring oscillator comprising a plurality of coupled stages, wherein:

each of the plurality of coupled stages for a first given ring oscillator comprises an inverter having at least one first MOS device having a first designed gate length;

each of the plurality of coupled stages for a second given ring oscillator comprises an inverter substantially identical to the inverters in the coupled stages of the first given ring oscillator and coupled to at least one second MOS device having a second designed gate length;

each of the plurality of coupled stages for a third given ring oscillator comprises an inverter substantially identical to the inverters in the coupled stages of the first given ring oscillator and coupled to at least one third MOS device having a third designed gate length;

the second and third designed gate lengths are different; and

one of the second and third designed gate lengths is substantially ~~approximately~~ equal to the first designed gate length;

determining performance by using at least one of the given ring oscillators; and

determining, using the plurality of ring oscillators, at least one additional characteristic of MOS devices in the plurality of ring oscillators.

2. (Original) The method of claim 1, wherein the step of determining performance further comprises the steps of causing the at least one given ring oscillator to oscillate so that a delay of a coupled stage in the at least one given ring oscillator is under 30 picoseconds.

3. (Currently Amended) The method of claim 1, wherein the predetermined distance is substantially ~~approximately~~ 1,000 microns or less.

4. (Original) The method of claim 1, wherein the plurality of ring oscillators are coupled together through circuitry.

5. (Original) The method of claim 1, wherein the at least one second MOS device comprises an NMOS gate and a PMOS gate coupled together in parallel, and wherein the at least one third MOS device comprises an NMOS gate and a PMOS gate coupled together in parallel.

6. (Original) The method of claim 1, wherein the plurality of ring oscillators comprise five ring oscillators, wherein the at least one second MOS device comprises at least one NMOS gate, wherein the at least one third MOS device comprises at least one NMOS gate, wherein each of the plurality of coupled stages for a fourth given ring oscillator comprises an inverter coupled to at least one first PMOS gate having a fourth designed gate length, and wherein each of the plurality of stages for a fifth given ring oscillator comprises an inverter coupled to at least one second PMOS gate having a fifth designed gate length, wherein the fourth and fifth designed gate lengths are different.

7. (Original) The method of claim 1, wherein the plurality of ring oscillators comprise a fourth given ring oscillator, wherein each of the plurality of stages for the fourth given ring oscillator comprises an inverter coupled to at least one fourth MOS device having a fourth designed gate length, wherein the fourth designed gate length is larger than the third designed gate length, and wherein the third designed gate length is larger than the second designed gate length.

8. (Original) The method of claim 7, wherein each of the at least one second, third and fourth MOS devices comprises at least one NMOS gate.

9. (Original) The method of claim 7, wherein each of the at least one second, third and fourth MOS devices comprises at least one PMOS gate.

10. (Original) The method of claim 1, wherein the step of determining at least one additional characteristic further comprises the steps of:

measuring a frequency of oscillation for each of at least the first, second, and third given ring oscillators of the plurality of ring oscillators;

determining delay for each of at least the first, second, and third given ring oscillators of the plurality of ring oscillators by using at least a corresponding one of the frequencies;

measuring active and quiescent current for each of at least the first, second, and third given ring oscillators of the plurality of ring oscillators;

determining load capacitance per stage for each of at least the first, second, and third given ring oscillators of the plurality of ring oscillators by using, for a respective one of the ring oscillators, at least the active and quiescent currents and delay.

11. (Original) The method of claim 10, wherein the step of determining at least one additional characteristic of MOS devices further comprises the step of determining physical gate length for a selected one of the given ring oscillators by using the designed gate length for the selected one of the ring oscillators and a bias length.

12. (Original) The method of claim 11, wherein the step of determining at least one additional characteristic of MOS devices further comprises the step of determining bias length by comparing capacitances determined for at least each of the first, second and third given ring oscillators with designed gate length for at least each of the first, second and third given ring oscillators.

13. (Original) The method of claim 11, wherein the selected one given ring oscillator is the third given ring oscillator, wherein the third designed gate length is greater than the second designed gate length, and wherein the step of determining at least

one additional characteristic of MOS devices further comprises the step of determining gate tunneling current per unit area by using at least the active current for the second and the third given ring oscillators and the designed gate lengths for the second and third given ring oscillators.

14. (Original) The method of claim 10, wherein the step of determining at least one additional characteristic of MOS devices further comprises the step of determining a thickness of oxide by using at least the load capacitance per stage for the second given ring oscillator and the load capacitance per stage for the third given ring oscillator.

15. (Original) The method of claim 10, wherein the step of determining at least one additional characteristic of MOS devices further comprises the step of determining an effective gate resistance by using at least the delays and capacitances for the first given ring oscillator and another of the given ring oscillators.

16. (Original) The method of claim 12, wherein the step of determining at least one additional characteristic of MOS devices further comprises the step of determining channel leakage current per unit width by using at least the gate tunneling current, the quiescent current for the first given ring oscillator and the physical gate length for the first given ring oscillator.

17. (Original) The method of claim 10, wherein the step of determining at least one additional characteristic of MOS devices further comprises the step of determining active power by using at least the active current and quiescent current for a selected one of the ring oscillators or by using the load capacitance and delay for a selected one of the ring oscillators.

18. (Original) The method of claim 10, wherein the step of determining at least one additional characteristic of MOS devices further comprises the

step of determining short circuit power at a supply voltage by using the load capacitance, the supply voltage, and the delay for a selected one of the ring oscillators.

19. (Currently Amended) An apparatus for determining characteristics of metal oxide semiconductor (MOS) devices, the apparatus comprising:

a plurality of ring oscillators, the plurality of ring oscillators located within a predetermined distance of each other, each ring oscillator comprising a plurality of coupled stages, wherein:

each of the plurality of coupled stages for a first given ring oscillator comprises an inverter having at least one first MOS device having a first designed gate length;

each of the plurality of coupled stages for a second given ring oscillator comprises an inverter substantially identical to the inverters in the coupled stages of the first given ring oscillator and coupled to at least one second MOS device having a second designed gate length;

each of the plurality of coupled stages for a third given ring oscillator comprises an inverter substantially identical to the inverters in the coupled stages of the first given ring oscillator and coupled to at least one third MOS device having a third designed gate length;

the second and third designed gate lengths are different; and

one of the second and third designed gate lengths is substantially ~~approximately~~ equal to the first designed gate length.

20. (Original) The apparatus of claim 19, wherein each ring oscillator comprises a frequency divider.

21. (Original) The apparatus of claim 19, wherein the ring oscillators are coupled together through circuitry.

22. (Original) The apparatus of claim 21, wherein the circuitry comprises a frequency divider coupled to each of the ring oscillators.

23. (Original) The apparatus of 19, wherein each of ring oscillators is coupled to an independent power supply, and wherein the circuitry is coupled to another independent power supply.

24. (Original) The apparatus of claim 23, wherein each independent power supply can be separately enabled.

25. (Original) The apparatus of claim 19, wherein the at least one second MOS device comprises an NMOS gate and a PMOS gate coupled together in parallel, and wherein the at least one third MOS device comprises an NMOS gate and a PMOS gate coupled together in parallel.

26. (Original) The apparatus of claim 19, wherein the plurality of ring oscillators comprise five ring oscillators, wherein the at least one second MOS device comprises at least one NMOS gate, wherein the at least one third MOS device comprises at least one NMOS gate, wherein each of the plurality of coupled stages for a fourth given ring oscillator comprises an inverter coupled to at least one first PMOS gate having a fourth designed gate length, wherein each of the plurality of coupled stages for a fifth given ring oscillator comprises an inverter coupled to at least one second PMOS gate having a fifth designed gate length, and wherein the fourth and fifth designed gate lengths are different.

27. (Original) The apparatus of claim 19, wherein the plurality of ring oscillators comprise a fourth given ring oscillator, wherein each of the plurality of coupled stages for the fourth given ring oscillator comprises an inverter coupled to at least one fourth MOS device having a fourth designed gate length, wherein the fourth designed gate length is greater than the third designed gate length, and wherein the third designed gate length is greater than the second designed gate length.

28. (Original) The apparatus of claim 27, wherein each of the at least one second, third and fourth MOS devices comprises at least one NMOS gate.

29. (Original) The apparatus of claim 27, wherein each of the at least one second, third and fourth MOS devices comprises at least one PMOS gate.

30. (Currently Amended) A mechanism ~~A semiconductor including at least one circuit~~ for determining characteristics of metal oxide semiconductor (MOS) devices~~, the~~ including at least one circuit comprising:

a plurality of ring oscillators, the plurality of ring oscillators located within a predetermined distance of each other, each ring oscillator comprising a plurality of coupled stages, wherein:

each of the plurality of coupled stages for a first given ring oscillator comprises an inverter having at least one first MOS device having a first designed gate length;

each of the plurality of coupled stages for a second given ring oscillator comprises an inverter substantially identical to the inverters in the coupled stages of the first given ring oscillator and coupled to at least one second MOS device having a second designed gate length;

each of the plurality of coupled stages for a third given ring oscillator comprises an inverter substantially identical to the inverters in the coupled stages of the first given ring oscillator and coupled to at least one third MOS device having a third designed gate length;

the second and third designed gate lengths are different; and

one of the second and third designed gate lengths is substantially ~~approximately~~ equal to the first designed gate length.

31. (Currently Amended) A method for determining characteristics of metal oxide semiconductor (MOS) devices, the method comprising the steps of:

determining performance by using at least one of a plurality of ring oscillators, the plurality of ring oscillators located within a predetermined distance of one another, each ring oscillator comprising a plurality of coupled stages, wherein:

each of the plurality of coupled stages for a first given ring oscillator comprises an inverter having at least one first MOS device having a first designed gate length;

each of the plurality of coupled stages for a second given ring oscillator comprises an inverter substantially identical to the inverters in the coupled stages of the first given ring oscillator and coupled to at least one second MOS device having a second designed gate length;

each of the plurality of coupled stages for a third given ring oscillator comprises an inverter substantially identical to the inverters in the coupled stages of the first given ring oscillator and coupled to at least one third MOS device having a third designed gate length;

the second and third designed gate lengths are different; and

one of the second and third designed gate lengths is substantially ~~approximately~~ equal to the first designed gate length; and

determining, using the plurality of ring oscillators, at least one additional characteristic of MOS devices in the plurality of ring oscillators.